UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,233	11/19/2001	Yvon Gris	S1022/8800	8198

23628 7590 08/09/2004

WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2211

EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/988,233	GRIS ET AL.	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-15,20-37,39-42 and 45-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-15,20-37,39-42 and 45-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 11 is rejected under 35 U.S.C. 102(b) as being anticipated by Shishiguchi (JP 9-64016), where US 5,821,158 is used as an accurate translation, or 35 U.S.C. 102(e) as being anticipated by Shishiguchi (US 5,821,158).

Shishiguchi discloses implanting germanium ions into a single crystalline silicon substrate ('158 col 6, ln 40-65 and claim 1), this reads on applicants' electrically neutral species because applicants teach germanium implants remain electrically neutral, note page 4 of the

instant specification. Shishiguchi also discloses after the implantation, Si_2H_6 is supplied to the to grow a silicon epitaxial film at 650°C ('158 col 6, ln 40-65).

Shishiguchi is silent to the implantation forms defects in a region of the substrate, however implantation inherently produces defects, as evidenced by applicants' specification, note page 4.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 11, 13-15, 21-24, 27-30, 32-37, 39-41, and 45-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) in view of Meyerson (US 5,298,452) or Kagata et al (US 5,221,412).

Takizawa et al discloses a Si substrate **11** grown a Czochralski method is dry oxidized at a temperature of 1000°C to form a SiO_2 film **13** on the surface of the substrate **11**. Takizawa et al also discloses carbon is ion-implanted into the substrate through the SiO_2 film **13** and the resultant structure is annealed in an N_2 atmosphere. Thereafter, the SiO_2 film is removed and a Si epitaxial layer **16** is grown at a temperature of about 1150°C (col 4, ln 15-65). Takizawa et al also discloses ion-implanting electrically neutral C, Ge, Sn, Pb or the like which are Group IV elements may be ion-implanted into the Silicon substrate **11** and an element other than a Group IV element may be ion-implanted into the substrate together with the Group IV element (col 6, ln 15-35).

Takizawa et al does not disclose depositing a silicon layer on the region at a temperature of less than 750°C.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr (1.3 to 0.013 Pa). Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Takizawa et al with Meyerson process of forming epitaxial silicon at reduced temperatures to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures and superior properties (col 17, ln 20-35).

In a method of growing Si single crystal films, note entire reference, Kagata et al teaches a vapor phase epitaxial growth of Si single crystal film having a less amount of stacking faults and a less amount of polycrystals produced on a Si single crystal substrate (col 1, ln 60 to col 2, ln 10). Kagata et al also teaches Si single crystal film deposition at 700°C or lower, specifically

550-680°C. Kagata et al also teaches the pressure may be normal or reduced to about 50 Torr but a pressure of 660-860 Torr near atmospheric pressure is preferred (col 3, ln 45-65). Kagata et al also teaches using disilane and hydrogen (col 2, ln 35-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Takizawa et al wit Kagata et al's process of forming single crystal silicon to form a single crystal film having less stacking faults and a less amount of polycrystals.

Referring to claims 13-15, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches silane and hydrogen at a pressure of 1.3 Pa and 50 Torr.

Referring to claims 21, 24, 39 and 41, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches removing an oxide layer and a thickness of 20 nm. The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al does not teach a thickness of less then 10 nm and depth of 5 nm or less. The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches the thickness of SiO_2 film can be reduced depending on the acceleration or dose of the implantation ('195 col 5, ln 1-5). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al by using an oxide thickness of less then 10 nm for a reduced implantation dose.

Referring to claim 22, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches ion-implantation, this reads on applicants' process that directs ions toward the region.

Referring to claims 23 and 40, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al does not teach the density of interstitial defects. The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al does teach crystal defects form in the substrate by implantation improve the gettering capability of the wafer ('195 col 6, ln 5-15), this is a teaching that the defects are result effective variables. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al by conducting routine experimentation to determine the optimum amount of interstitial defects per one hundred silicon atoms.

Referring to claims 27 and 32, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al is silent to the silicon layer is deposited with a different orientation than that of the substrate. However, since the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches a similar method as claimed, under the principle of inherency the invention is considered to be anticipated by the combination of Takizawa et al and Meyerson.

Referring to claim 29, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al is silent to the crystallinity of the substrate. However, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches a substrate formed by the Czochralski process. The Czochralski process inherently produces substrate with single crystalline orientation, as evidenced by Matsuo et al (US 4,515,755) below.

Referring to claim 30, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al inherently teach a single crystalline Silicon substrate, as discussed previously; therefore an epitaxial silicon grown on a single crystalline substrate will inherently be single crystalline.

Referring to claim 45-46, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al does not teach the pressure. The combination of Takizawa et al and Kagata teach pressures from 50 Torr to 1 atm. Overlapping ranges are held to be obvious (MPEP 2144.05). Furthermore, pressure is well known to be a result effective variable. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Kagata et al by optimizing pressure by conducting routine experimentation of a result effective variable (MPEP 2144.05).

Referring to claims 49-50, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches carbon, this reads on applicants' atoms.

Referring to claims 47-48 and 51-52, the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches a temperature of less then 800°C, specifically 550°C. Overlapping ranges are held to be obvious (MPEP 2144.05).

5. Claims 11-15, 22-23, 27-28, 45, 47, 49, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goesele et al (US 5,024,723) in view of Meyerson (US 5,298,452) or Kagata et al (US 5,221,412).

Goesele et al teaches the formation of an epitaxial silicon layer on a silicon substrate after a low energy low dose carbon implantation, this reads on applicants' electrically neutral species

because carbon has the similar electrical properties as silicon because carbon has the same number of valence electrons as silicon and both silicon and carbon are Group IVB elements. Goesele et al also teaches after growing an epitaxial silicon layer the wafer is annealed (claim 9 and col 3, ln 5 to col 4, ln 15).

Goesele et al is silent to the temperature of the epitaxial silicon deposition is less than 750°C.

Meyerson teaches a method of forming epitaxial silicon using silane and a hydrogen carrier gas at a growth temperature of less than 800°C at a pressure of 10^{-2} to 10^{-4} Torr (1.3 to 0.013 Pa). Meyerson also teaches excellent uniformity is obtained across the wafer because of the low pressure (col 9, ln 9-60). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Goesele et al with Meyerson process of forming epitaxial silicon at reduced temperatures to form an epitaxial silicon layer with excellent uniformity at reduced operating temperatures and superior properties (col 17, ln 20-35).

In a method of growing Si single crystal films, note entire reference, Kagata et al teaches a vapor phase epitaxial growth of Si single crystal film having a less amount of stacking faults and a less amount of polycrystals produced on a Si single crystal substrate (col 1, ln 60 to col 2, ln 10). Kagata et al also teaches Si single crystal film deposition at 700°C or lower, specifically 550-680°C. Kagata et al also teaches the pressure may be normal or reduced to about 50 Torr but a pressure of 660-860 Torr near atmospheric pressure is preferred (col 3, ln 45-65). Kagata et al also teaches using disilane and hydrogen (col 2, ln 35-40). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Goesele et al with Kagata

et al's process of forming single crystal silicon to form a single crystal film having less stacking faults and a less amount of polycrystals.

Referring to claim 11, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches implantation caused crystal damage (col 3, ln 5-15), this reads on applicants' defects.

Referring to claim 12, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches epitaxial deposition then annealing, note Goesele et al (claim 9).

Referring to claims 13-15, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches silane and hydrogen at a pressure of 1.3 Pa and 50 Torr.

Referring to claim 22, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches direction carbon ions to the silicon substrate.

Referring to claim 23, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al is silent forming to the interstitial defect in the region with an atomic proportion of one defect per one hundred silicon atoms. The combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al does teach temperature will lower the rate of implantation caused crystal damage in the substrate, which suggests reducing crystal damage. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al by optimizing the defects to obtain same by conducting routine experimentation of a result effective variable.

Referring to claim 27, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al is silent to the orientation of the silicon layer and the substrate. The substrate and the silicon layer inherently have different orientation because the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teach implanting a silicon substrate with carbon, which will inherently change the orientation of the surface silicon substrate. Therefore, an epitaxial silicon thereon will mimic the orientation of the modified surface of the substrate, which will inherently be different from the substrate originally. Furthermore, applicants teach the silicon is formed with a different orientation by implanting ions and depositing silicon without annealing, which is similar to the method taught by the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al.

Referring to claim 28, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches a silicon substrate.

Referring to claim 45, the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al does not teach the pressure. The combination of Goesele et al and Kagata teach pressures from 50 Torr to 1 atm. Overlapping ranges are held to be obvious (MPEP 2144.05). Furthermore, pressure is well known to be a result effective variable. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Goesele et al and Kagata et al by optimizing pressure by conducting routine experimentation of a result effective variable (MPEP 2144.05).

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) in view of Meyerson (US 5,298,452) or Kagata et al (US 5,221,412), as applied to claims 11, 13-15, 21-24, 27 and 29 above, and further in view of Wu et al (US 4,584,026).

The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teaches using electrically neutral elements into a silicon substrate. The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al does not teach using fluorine.

In a method of ion-implantation of phosphorus, arsenic or boron, note entire reference, Wu et al teaches implanting fluorine ions and then implanting phosphorus, arsenic or boron because double implanted wafers reached a useful level of conductivity at lower temperatures (col 5, ln 1-30). Wu et al also teaches fluorine ions are electrically inert (col 3, ln 20-30 and col 4, ln 5-20), this reads on applicants' implanting electrically neutral species and this is a teaching that fluorine is acceptable as an electrically neutral species. It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al with Wu et al's fluorine implant because substitution of a known material based on its suitability is held to be obvious (MPEP 2144.07).

7. Claims 29-30, 32-37, 40, and 45-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goesele et al (US 5,024,723) in view of Meyerson (US 5,298,452) or Kagata et al (US 5,221,412) as applied to claims 11-15, 22, and 27-28 above, and further in view of Yoshino (US 5,561,076).

The combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches all of the limitations of claim 29, as discussed previously, except the substrate is a single crystal.

In a method of forming a device on a silicon-on-insulator (SOI) structure, Yoshino teaches a typical SOI wafer has a single crystal silicon substrate, a silicon dioxide film laid on top of the upper surface of the silicon substrate and a single crystal silicon layer laid on top of the upper surface of silicon dioxide (col 1, ln 25-40).

The combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al does teach forming a silicon-on-insulator structure ('723 col 1, ln 5-10) and is not particular to the crystallinity of the silicon substrate ('723 claim 9). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al by using a conventional single crystal silicon substrate, as taught by Yoshino.

Referring to claim 32, the combination of Goesele et al, Meyerson and Yoshino or the combination of Goesele et al, Kagata et al and Yoshino teaches implanting carbon into a single crystal silicon substrate and then performing single crystal epitaxial silicon deposition on the damaged substrate, as applicants; therefore the single crystal silicon layer inherently has a different orientation than the undamaged silicon single crystal substrate.

8. Claims 25-26 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) in view of Meyerson (US 5,298,452) or Kagata et al (US 5,221,412), as applied to claims 11, 13-15, 21-24, 27 and 29 above, and further in view of

Tihanyi et al (US 3,897,625) or Takiyama et al (JP 8-8262), an English Abstract has been provided.

The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al teach all of the limitations of claim 25, as discussed previously, except forming a window in a layer on the substrate to expose the region.

In a method of selective gettering, note entire reference, Tihanyi et al teaches making a field effect transistor having a short channel length by forming a protective covering layer on a silicon layer that can be gettered, removing portions of the protective layer and forming a gettering layer on the exposed silicon surface (Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata's gettering with Tihanyi et al selective gettering using a protective layer to form a useful field effect transistor device.

In a method of manufacturing a semiconductor device, Takiyama et al teaches using silicon nitride film as a mask to form and implanting carbon to form gettering sites in a silicon substrate (Abstract). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata's gettering with Takiyama et al mask so as to gettering in a selective manner, thereby forming a useful semiconductor device.

Referring to claim 26, the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama et al or the combination of Takizawa et al, Kagata et al and Tihanyi et al or the combination of Takizawa et al, Kagata et al and Takiyama et al is silent to the width of the window. The dimensions of a mask are well

known in the art to be directly related to characteristic features of the semiconductor device produced and smaller devices are well known to be advantageous. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Takizawa et al, Meyerson and Tihanyi et al or the combination of Takizawa et al, Meyerson and Takiyama et al by optimizing the width of the protective layer by conducting routine experimentation (MPEP 2144.05).

9. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takizawa et al (US 5,734,195) or Goesele et al (US 5,027,723) in view of Meyerson (US 5,298,452) or Kagata et al (US 5,221,412), as applied to claim 11 above, and further in view of Candelaria (US 5,441,901).

The combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al or the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al teaches all of the limitations of claim 11, as discussed previously, except the region comprises an emitter of a bipolar transistor.

In a method of making a semiconductor device, Candelaria teaches a silicon semiconductor layer forms an emitter region in a heterojunction bipolar transistor device (claim 1; col 2, ln 20-45 and col 4, ln 40-50). It would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the silicon layer taught by the combination of Takizawa et al and Meyerson or the combination of Takizawa et al and Kagata et al or the combination of Goesele et al and Meyerson or the combination of Goesele et al and Kagata et al by forming an emitter to be useful in a semiconductor device.

Response to Arguments

10. Applicant's arguments, see page 6 of applicants remarks, filed 5/24/2004, with respect to claims 11-15, 20-37, 39-42 and 47-48 have been fully considered and are persuasive. The rejection of claims 11-15, 20-37, 39-42 and 47-48 has been withdrawn.

11. Applicant's arguments with respect to claims 11-15, 20-37, 39-42 and 45-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Plumton (US 5,554,561) teaches that doping by implantation affects the crystal orientation of GaAs grown on GaAs (col 1, ln 60-67 and col 7, 50-67).

Burns et al (US 5,011,789) teaches growing a single crystal Si film at 650-800°C at a pressure of 6 Pa and the importance of low temperatures to prevent transfer of dopants (col 3, ln 35 to col 4, ln 15 and col 6, ln 1-5).

Matsuo et al (US 4,515,755) teaches a well known method of manufacture of silicon single crystals used as wafers for semiconductor devices is the Czochralski method (col 1, ln 5-40).

Mochizuki et al (JP 2-044714) teaches ion-implanting germanium into a silicon single crystal substrate and depositing a silicon thereon followed by annealing the film (Abstract).

Kurogi et al (US 4,637,127) teaches a silicon single crystal substrate used in CMOS (col 11, ln 10-20).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER